

What is claimed is:

1           1. A field effect transistor comprising, in  
2 combination:  
3               a) a substrate having a substantially-planar  
4 upper substrate surface;

5               b) an elongated channel of semiconductor  
6 material, said elongated channel being inclined with  
7 respect to said upper substrate surface;

8               c) said channel including a top and a bottom  
9 with the bottom of the channel contacting said upper  
10 substrate surface;

11              d) said substrate being substantially  
12 conductive in the region contacting said bottom of said  
13 elongated channel;

14              e) said channel including a heavily doped  
15 region adjacent the top thereof; and

16              f) a gate comprising a planar layer of  
17 conductive material arranged substantially parallel to  
18 said upper substrate surface.

1           2. A field effect transistor as defined in  
Claim 1 further including a gate insulator layer  
substantially surrounding the length of said elongated  
channel.

1           3. A field effect transistor as defined in  
Claim 1 further including a first substantially-planar  
insulating layer between said gate and said upper  
substrate surface.

1           4. A field effect transistor as defined in  
Claim 3 further including a second substantially-planar  
insulating layer overlying said gate.

1               5. A field effect transistor as defined in  
2 Claim 2 further including a layer of conductive  
3 material in contact with said gate and substantially  
4 surrounding the length of said elongated channel.

1               6. A field effect transistor as defined in  
2 Claim 1 wherein said substrate is of semiconductor  
3 material.

1               7. A field effect transistor as defined in  
2 Claim 6 wherein said semiconductor material is globally  
3 moderately-doped and includes a locally highly-doped  
4 region adjacent the bottom of said elongated channel.

1               8. A field effect transistor as defined in  
2 Claim 6 wherein said semiconductor material is globally  
3 heavily-doped.

1               9. A field effect transistor as defined in  
2 Claim 1 wherein said elongated channel comprises  
3 silicon.

1               10. A field effect transistor as defined in  
2 Claim 1 further characterized in that:

3               a) said substrate comprises single crystal  
4 silicon; and

5               b) said elongated channel comprises silicon  
6 epitaxially grown from said substrate.

1               11. A field effect transistor as defined in  
2 Claim 1 wherein said elongated channel is substantially  
3 orthogonal to said upper substrate surface.

1               12. A method for forming a field effect  
2               transistor comprising the steps of:  
3               a) providing a conductive substrate; then  
4               b) etching said substrate to form an  
5               upstanding pillar adjacent a substantially-planar upper  
6               surface of said etched substrate; then  
7               c) forming a stack of substantially-planar  
8               layers of material adjacent said pillar, said stack of  
9               material comprising a first insulator layer adjacent  
10              said upper surface of said etched substrate, a gate  
11              layer of conductive material overlying said first  
12              insulator layer and a second insulator layer overlying  
13              said gate layer; then  
14              d) etching said pillar to the level of said  
15              substantially-planar upper surface of said etched  
16              substrate to form a upstanding pore within said stack;  
17              then  
18              e) forming a gate insulator layer at the  
19              interior of said upstanding pore; then  
20              f) forming an upstanding channel of  
21              semiconductor material having a top region and a bottom  
22              region interior of said gate insulator layer; and then  
23              g) heavily doping said top region of said  
24              upstanding channel of semiconductor material.

1               13. A method as defined in Claim 12 wherein  
2               the step of etching said substrate further includes the  
3               steps of:  
4               a) masking said substrate with a  
5               nanoparticle; and then  
6               b) directionally etching said masked  
7               substrate whereby whereby said pillar is a nanopillar  
8               and said pore is a nanopore.

1               14. A method as defined in Claim 13 further  
2               including the step of depositing a layer of conductive  
3               material in contact with said gate layer at the  
4               interior of said nanopore.

1               15. A method as defined in Claim 13 further  
2               characterized in that the step of forming an upstanding  
3               channel of semiconductor material further includes the  
4               step of epitaxially growing said channel from said  
5               substrate.

1               16. A method as defined in Claim 15 wherein  
2               said substrate comprises single crystal silicon.

1               17. A method as defined in Claim 13 wherein  
2               said substrate comprises a highly-doped semiconductor  
3               material.

1               18. A method as defined in Claim 17 wherein  
2               said substrate comprises highly-doped silicon.

1               19. A method as defined in Claim 12 wherein  
2               said gate layer comprises a metal.

1               20. A method as defined in Claim 12 wherein  
2               said gate layer comprises a highly-doped semiconductor.

1               21. A method for forming a field effect  
2               transistor comprising the steps of:  
3               a) providing a substrate of semiconductor  
4               material; then  
5               b) etching said substrate to form an  
6               upstanding pillar, adjacent a substantially-planar upper  
7               surface of said etched substrate; then  
8               c) creating a conductively-doped region  
9               within said etched substrate substantially and  
10              immediately beneath said pillar; then  
11              d) forming a stack of substantially-planar  
12              layers of material adjacent said pillar, said stack of  
13              materials comprising a first insulator layer adjacent  
14              said upper surface of said etched substrate, a gate  
15              layer of conductive material overlying said first  
16              insulator layer and a second insulator layer overlying  
17              said gate layer; then  
18              e) etching said pillar to the level of said  
19              substantially-planar upper surface of said etched  
20              substrate to form an upstanding pore within said stack;  
21              then  
22              f) forming a gate insulator layer interior to  
23              said upstanding pore; then  
24              g) forming an upstanding channel of  
25              semiconductor material having a top region and a bottom  
26              region interior of said gate insulator layer; and then  
27              h) heavily doping said top region of said  
28              upstanding channel.

1           22. A method as defined in Claim 21 wherein  
2       the step of etching said substrate further includes the  
3       steps of:

4           a) masking said substrate with a  
5       nanoparticle; and then

6           b) directionally etching said masked  
7       substrate whereby whereby said pillar is a nanopillar  
8       and said pore is a nanopore.

1           23. A method as defined in Claim 22 further  
2       including the step of depositing a layer of conductive  
3       material in contact with said gate layer at the  
4       interior of said nanopore.

1           24. A method as defined in Claim 22 further  
2       characterized in that the step of forming an upstanding  
3       channel of semiconductor material further includes the  
4       step of epitaxially growing said channel from said  
5       substrate.

1           25. A method as defined in Claim 24 wherein  
2       said substrate comprises single crystal silicon.

1           26. A method as defined in Claim 21 wherein  
2       said gate layer comprises a metal.

1           27. A method as defined in Claim 21 wherein  
2       said gate layer comprises a highly-doped semiconductor.

1               28. A method for forming a field effect  
2               transistor comprising the steps of:  
3               a) providing a substrate having an upper  
4               surface; then  
5               b) forming a stack of substantially-planar  
6               layers of material on said substrate, said stack  
7               comprising a first insulator layer adjacent said upper  
8               surface of said substrate, a gate layer of conductive  
9               material overlying said first insulator layer and a  
10              second insulator layer overlying said gate layer; then  
11              c) forming an overlayer on top of said second  
12              insulator layer; then  
13              d) masking said overlayer with a  
14              nanoparticle; then  
15              e) directionally etching said overlayer to  
16              form an upstanding nanopillar on top of said second  
17              insulator layer; then  
18              f) depositing a second overlayer on top of  
19              said second insulator layer and said upstanding  
20              nanopillar; then  
21              g) removing said second overlayer to the top  
22              of said upstanding nanopillar; then  
23              h) removing said nanopillar to leave an upper  
24              nanopore within said second overlayer defining an etch  
25              mask; then  
26              i) directionally etching a lower nanopore to  
27              said upper surface of said substrate; then  
28              j) removing said second overlayer; then  
29              k) forming a gate insulator layer at the  
30              interior of said upstanding nanopore; then  
31              l) forming an upstanding channel of  
32              semiconductor material having a top region and a bottom  
33              region interior of said gate insulator layer; and then  
34              m) heavily doping said top region of said

35 upstanding channel of semiconductor material.

36           29. A method as defined in Claim 28 further  
37           including the step of depositing a layer of conductive  
38           material in contact with said gate layer at the  
39           interior of said nanopore.

1           30. A method as defined in Claim 28 further  
2           characterized in that the step of forming an upstanding  
3           channel of semiconductor material further includes the  
4           step of epitaxially growing said channel from said  
5           substrate.

1           31. A method as defined in Claim 30 wherein  
2           said substrate comprises single crystal silicon.

1           32. A method as defined in Claim 28 wherein  
2           said gate layer comprises a metal.

1           33. A method as defined in Claim 28 wherein  
2           said gate layer comprises a highly-doped semiconductor.